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Settling Time of Operational Amplifiers

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FOREWORD

It is possible to measure voltages and currents to within small (even fractional) parts per million, traceable all the way to the Bureau of Standards. Typically, at the limits of precision, repeated measurements must be made over a period of time, after which an experienced practitioner can state with a great deal of certainty that a voltage or a current had, during that interval, an average value expressible to six or more significant figures.

That this can be accomplished is interesting, impressive, and of basic importance to all engineers, but it is of little direct relevance to a far more pervasive type of measurement. This is the measurement that calls for a more modest degree of accuracy – four significant figures at best (today), but the measurement must be completed, often within a microsecond or so, then converted, stored, and utilized by a computer. The time taken to complete the measurement to the desired degree of accuracy, be it ±1%, ±0.1%, ±0.01%, or ±½LSB, in terms of its final value (with the often-added provision that said final value is within a similarly small fraction of full scale of its nominal expected value) is usually called Settling Time. This interval may be quite short: at present ±0.01% within 0.5 to 1.0 microseconds is fashionable; next year engineers will consider an order of magnitude improvement in performance feasible (and many will attain it). Significant improvements will be reported in these pages.

The purpose of the present discussion is to provide an interpretation of Settling Time, and to set before the engineer the issues involved in terms of circuit design, hardware, specifications, applications, and measurements. We shall try, to the degree possible, to avoid the use of intimidating mathematical formulae, and to reveal practical circuits and mathematical shortcuts.

INTRODUCTION

Much has been written on the subject of small-signal frequency response characteristics of amplifiers; and most users of operational amplifiers are able to make use of the manufacturers' specifications to calculate closed-loop bandwidth, analyze stability, determine phase errors, etc.[1] Most manufacturers also provide data sufficient to characterize the full power response and slew rate of the amplifier.

[1] Footnote references are to numbered items in the bibliography, page 11.

The important difference of Settling Time investigations is that, although frequency response may be a tool, the results must be either implicitly or (preferably) explicitly measurable in the Time Domain. They are in general terribly nonlinear and subject to (so it would seem) every stray nastiness that Nature has evolved, because of the combined stress on both speed and accuracy.

Thus the recently-increased use of operational amplifiers in handling data in systems calling for high-speed switching rates, especially in connection with digital computers, has led to a requirement for *time-response* characterization of general- and special-purpose operational amplifiers. A typical problem is the application of rapidly-changing signals (e.g., step functions) to a buffer amplifier, which must faithfully reproduce the input to a high degree of accuracy within a period of the order of a microsecond. This requires that the amplifier be designed and optimized for *Settling Time*. Applications requiring fast settling time to high accuracies are typified by Sample-Hold circuits, Multiplexers, and amplifiers used with A/D and D/A converters. Settling time is important in these applications because it is the principal factor which determines the maximum data or information transfer rate for a given accuracy. A tradeoff is generally possible between data rate and accuracy: viz., higher data rates are possible at the sacrifice of accuracy. It should also be noted that the buffer amplifier, as but one step in a process, is now one of the major limitations on system speed.

DEFINITION

SETTLING TIME *is the time elapsed from the application of an ideal instantaneous step input to the time at which the closed-loop amplifier output has entered and remained within a specified error band, usually symmetrical about the final value. Settling time includes a very brief propagation delay, plus the time required for the output to slew to the vicinity of*

(Continued on p. 2)

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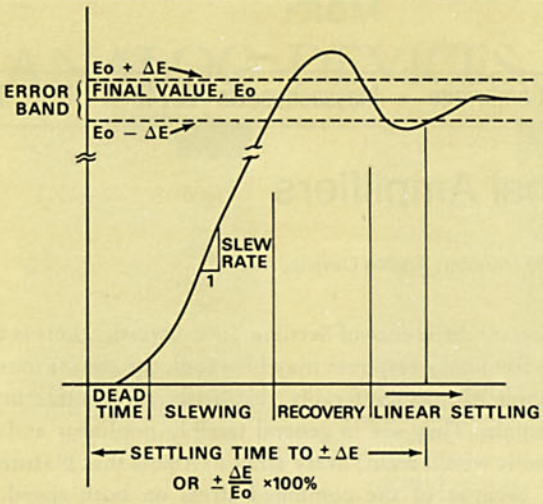
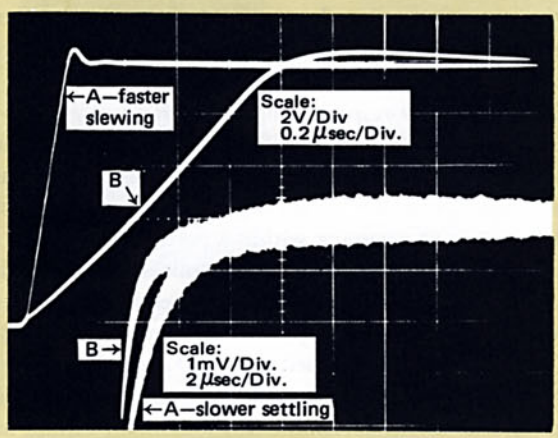
DEFINITION *(Continued from p. 1)*

the final value, recover from the overload condition associated with slewing, and finally settle to within the specified error. Figure 1 illustrates this definition of Settling Time.



(a) Components of settling time (nonlinear scale)



(b) Annotated wave forms illustrating comparative settling time of two typical op amps.

Figure 1. Pictorial Definition of Settling Time

CAUTION: The above definition has been used widely in the data acquisition field for at least the past 10 years. Nevertheless, some manufacturers new to this field (but not to the tricks of "specmanship") define "settling time" as the time required to settle within the linear small-signal region only. When considering the products and applications literature of these manufacturers, it is important to realize that their term usually corresponding to Settling Time is "Acquisition Time." (Until adopted for this usage, Acquisition Time had a specialized meaning of its own: minimum time required for a Sample-Hold switch to be closed to allow re-opening without loss of information, usually without the necessity that the amplifier finish settling.) We do not know at present what standards will eventually emerge, but we shall always identify small-signal settling time by attaching the "small signal" label wherever it would be misleading to do otherwise.

Settling time may also be defined in terms of the recovery time of the amplifier from an instantaneous error caused by a step or an impulse change in load. Because Settling Time is determined by a combination of amplifier characteristics, nonlinear as well as linear, and because it is a closed-loop parameter, it cannot readily be predicted from such open-loop specifications as slew rate, small-signal bandwidth, etc.

Two frequently-occurring applications requiring fast settling time for maximum transfer rate are indicated in Figures 2 and 3. Figure 2 depicts the typical Multiplexer problem (only two channels shown, for simplicity). One line is at 0V, the other is at -10V. When switching from one channel to the other, the amplifier's input may be subjected to a 10-volt step and must recover to the millivolt level in high-accuracy systems. Figure 3 indicates a typical waveform from a high-speed D/A Converter (DAC) showing large transient spikes ("glitches") caused by time skew between turn-on and turn-off of the DAC's switches. The settling time of the amplifier used (if the DAC uses an amplifier) limits the maximum bit rate for an A/D Converter (ADC) using the DAC.

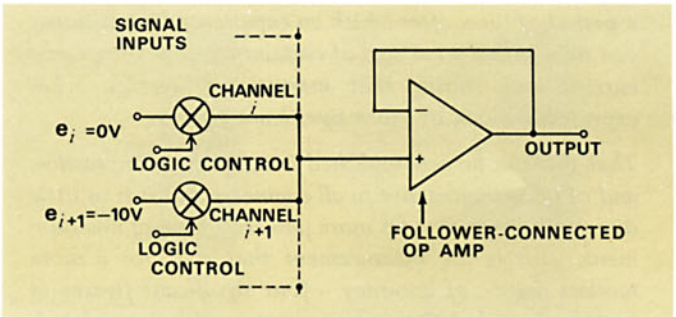


Figure 2. Simplified diagram of muliplexer circuit

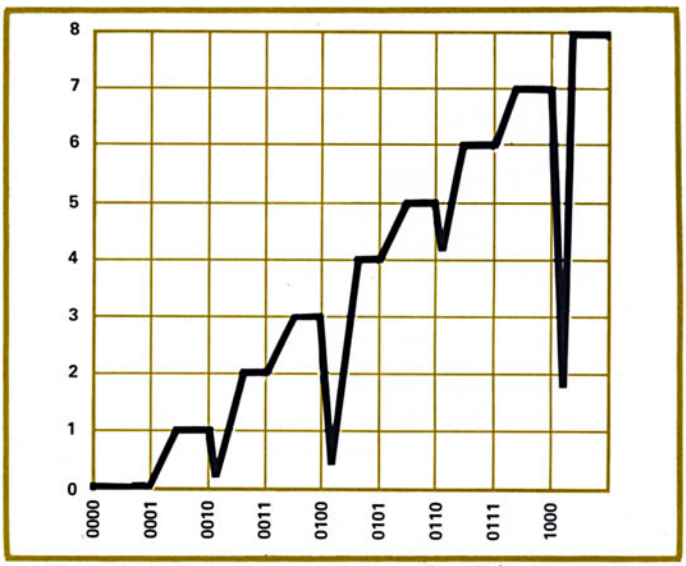


Figure 3. Output of counter-driven Fast D/A Converter showing "glitches"

AMPLIFIER DESIGN FACTORS AFFECTING SETTLING TIME

The design factors to be discussed here are those that the amplifier designer and the engineer who specifies the amplifier must consider. Other design factors concerning the circuit the amplifier is tested or used in will be discussed in a later section.

LINEAR OPERATING RANGE. Although the essence of the problem of settling time is nonlinear, the factors to be discussed in this section pertain to the all-important linear-settling "tail", which applies to both small signals and large (though not always identically). "Linear" means that the amplifier and all associated elements are operating in the linear range, i.e., the parametric relationship is independent of voltage or current level, or its previous history.

Noise. The amplifier's output can never settle within a given band of error if its output noise, however generated, is comparable to the magnitude of the band defined for settling. In addition to inherent amplifier circuit noise, the designer must also consider the effects of interference noise, whether coupled from the external environment, the power supply, the input signal, or the logic signals in the associated circuitry. For a discussion of noise in operational amplifier circuits, see *Analog Dialogue,* Vol. 3, No. 1.

DC Gain. To ensure the accuracy of the final value, the gain of an amplifier which must settle to within ±0.01% should be at least 10,000 for unity-gain followers, 20,000 for unity gain inverters, and more for higher-closed-loop-gain amplifiers. If the amplifier's open-loop input-output characteristic is reasonably linear, the error caused by slightly-lower gains may be compensated for under a given set of conditions by trimming the feedback ratio. For follower applications, the CMRR should be commensurate with the desired gain accuracy.

Drift and Offset. For high-precision applications, offset must be low or adjustable, and drift over the temperature range should be within the error corresponding to the desired accuracy. For example, ±0.01% error in ±10V circuitry requires less than ±1 millivolt (±½mV in inverter applications). Bias current drift may not be disregarded: 1 millivolt in 10kΩ requires that bias current change less than 100 nanoamperes.

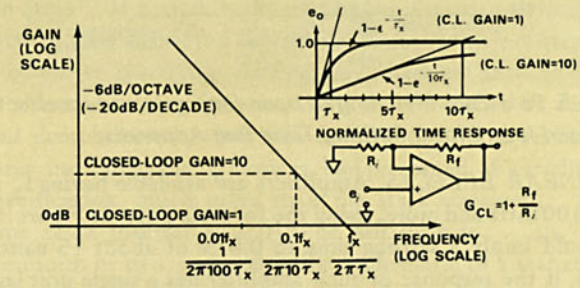
Dynamic Stability. Operational amplifiers designed for "optimum" response at high gains at low frequency often have transfer functions that provide only marginal stability when the loop is closed more tightly for near-unity gain and wide bandwidth. The amplifier used for fast settling to high accuracy should have a closed-loop response that is (at least theoretically) not much worse than critically-damped, as any oscillation or ringing may prolong settling time. Furthermore, in practical circuits, which have stray capacitance, the added lags caused by the external loop elements will cause an amplifier having insufficient phase margin to ring. For this reason, designers of fast-settling operational amplifiers strive to have the open-loop frequency characteristic be strongly dominated by a single time constant. This is stated in many ways, all having the same meaning: constant 90° phase shift, -6dB/octave (or -20dB/decade) rolloff, unit lag, exponential response, etc.

Amplifiers characterized by this form of response may be considered to be integrators with limited DC gain, characterized by the following equation:*

$$A_{OL} = \frac{1}{\tau_x p}\left[\frac{A_0 \tau_x p}{1 + A_0 \tau_x p}\right] \cong \frac{1}{\tau_x p} \cong -j\frac{f_x}{f}$$

*Note: p is the Heaviside differentiation operator, corresponding roughly to s or jω, A_{OL} is open-loop gain, A_0 is DC gain, f_x is unity gain bandwidth, $\tau_x = 1/2\pi f_x$

For many non-state-of-the-art applications, the single time constant response has the further advantage of being calculable virtually by inspection. Small-signal settling time of amplifiers with more complex transfer functions does not lend itself to ready calculation. Figure 4 shows the open- and closed-loop response of an amplifier having this popular characteristic, and provides a table indicating the relationship between small-signal settling time and amplifier unity-gain bandwidth (f_x) or characteristic time (τ_x).



(a) Bode (amplitude vs. frequency) Plot, Feedback Circuit, Time Response

Percent error	$T_s = -2.303\tau_x \log_{10}\eta$ for τ_x (μs) or f_x(MHz)			
	Gain = 1		Gain = 10	
100η	T_s vs. τ_x (μs)	T_s vs. f_x	T_s vs. τ_x	T_s vs. f_x
10 %	$2.303\tau_x$	$0.367/f_x$	$23.03\tau_x$	$3.67/f_x$
1.0 %	$4.606\tau_x$	$0.734/f_x$	$46.06\tau_x$	$7.34/f_x$
0.1 %	$6.909\tau_x$	$1.101/f_x$	$69.09\tau_x$	$11.01/f_x$
0.01%	$9.212\tau_x$	$1.468/f_x$	$92.12\tau_x$	$14.68/f_x$

(b) Settling Time vs. Fractional Error η for First-order Step Response as a Function of Open-Loop Characteristic Time (τ_x) or Unity-gain Bandwidth (f_x)

Figure 4. Closed-loop Response of Amplifier having -6dB/Octave Open-Loop Amplitude Response

Well-Behaved Dynamic Response. Multistage amplifiers require the matching of poles and zeros in the linear transfer function to achieve a 6dB/octave characteristic.[2,3] That is, m = 1 in the general expression:

$$A_{OL} = \frac{1}{\tau_x p}\left[\frac{A_0 \tau_x p}{1 + mA_0 \tau_x p}\right]\left[\frac{1 + mA_1 \tau_x p}{1 + A_1 \tau_x p}\right]$$

If the mismatch term, m, is substantially different from 1.0, and if A_1 is substantially less than the open-loop gain required for the desired degree of accuracy, the output of the amplifier will settle rapidly to within a small fraction (about $1/A_0$) of the final value, undershooting if m>1, overshooting if m<1, then settle exponentially to the final value with a surprisingly long time constant. (Fig. 5) The details of this consideration are described, and illustrated by scope pictures of the response of a low-speed dynamic model in the Appendix on pages 10 and 11.

Propagation Delay. At frequencies substantially beyond f_x, the amplifier's open-loop response starts to roll off more steeply and with greater phase shifts. The time-domain analogy to this is a brief interval of "dead time" of the order of nanoseconds, small compared to τ_x if the circuit is to be stable closed-loop. Because τ_x itself is not usually a limiting factor on settling time, propagation delay is even less so, in linear operation.

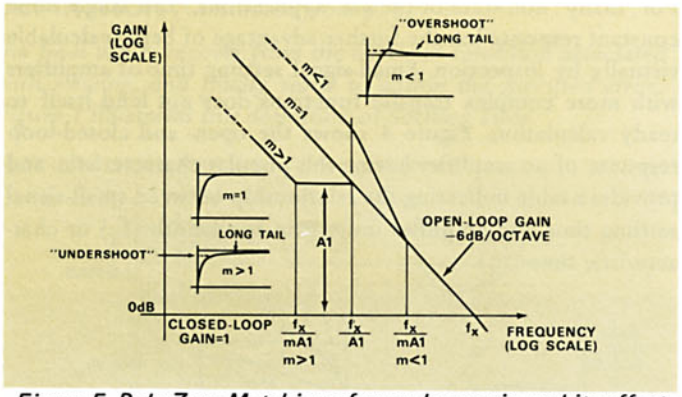


Figure 5. Pole-Zero Matching of open-loop gain and its effect on Closed-loop Linear Settling Time (see Appendix)

NONLINEAR EFFECTS. Amplifiers are available having f_x as high as 100 MHz and more. Using the formula given in Figure 4, this would imply a settling time to 0.01% of about 15 nanoseconds, if the response of such amplifier has a single unit-lag. Yet the specifications are more like 0.5 to 1.0 microseconds and more. Why? Here are some of the considerations:

Slew Rate. Within the amplifier, there are inherent semiconductor and circuit capacitances, as well as those added for stabilization; at the output, there is load capacitance. The rate of change of voltage at each point in the circuit is limited by the available current to charge the capacitance at that point ($dv/dt_{max}=I_{max}/C$). In the above example, if the amplifier were operating linearly over its whole output range, the initial rate of rise in response to a step would have to be 10V/1.6ns = 6,280 volts per microsecond! In order to drive a 10pF load without saturating, at least 62.8mA must be available.

ΔE	f_x(MHz)				τ_x (ns)				
	0.1	1.0	10	100	3.2	10	100	1000	10μs
10V	6.3	63	630	6,300	3,100	1000	100	10	1.0
5V	3.1	31	310	3,100	1,550	500	50	5	0.5
2V	1.3	13	130	1,300	620	200	20	2	0.2
1V	0.6	6	60	600	310	100	10	1	0.1

TABLE 1 — First-Order Response: Required Initial Rate of Change (Volts/μs) as a Function of Step Size, f_x, and τ_x.

$$\left[\frac{de}{dt}\right]_{max} = \frac{\Delta E}{\tau_x} = \Delta E\, 2\pi f_x$$

C ↓ de/dt →	1	10	20	50	100	200	500	1000
10pF	10μA	0.1	0.2	0.5	1.0	2.0	5.0	10.
20pF	20μA	0.2	0.4	1.0	2.0	4.0	10.	20.
50pF	50μA	0.5	1.0	2.5	5.0	10.	25.	50.
100pF	0.1	1.0	2.0	5.0	10.	20.	50.	100.
200pF	0.2	2.	4.0	10.	20.	40.	100.	200.
500pF	0.5	5.	10.	25.	50.	100.	250.	500.

TABLE II — Current (mA) to Maintain a Given Slew Rate (V/μs) As a Function of Capacitance. $\left[i = C\frac{de}{dt}\right]$

Tables I and II show the relationships between step size, slew rate required for exponential response, capacitor size, and required driving current, for a somewhat less exotic selection of parametric values. Table I gives examples of the slew rate requirement for linear behavior (i.e., exponential time response) as a function of step size and either f_x or τ_x, and Table II indicates the current required to drive a given capacitive load at the appropriate value of slew rate. In practice, such slew rates (in relation to small-signal frequency response) cannot be achieved: the excessive currents required would degrade accuracy and drift specifications; also the operational amplifier would be required to respond linearly to 100% error at its input (i.e., full-scale differential input). Typically, then, the amplifier slews, at a maximum rate 5 to 100 times less than that implied by its small signal bandwidth, up to the vicinity of full scale, recovers, and settles exponentially (either aperiodically or with oscillations).

Recovery. During nonlinear slewing, saturation imposes charge changes away from normal operating values on the circuit capacitances (including minority carrier storage in semiconductors). These must be discharged back to equilibrium values before the amplifier can operate normally. Thus, there is a period of recovery which is comparable to the period of slewing, but it may be substantially greater if many internal stages are involved. Fast slew rate, therefore, is not by itself a good indicator of a fast-settling amplifier. Some amplifiers with extremely-large slew rates have excessive recovery time and greater overall settling time than other amplifiers having more modest slew rates. In Figure 6, the Model 1011 tested has a slew rate of 70V/μs, but settles to 0.01% in 6μs, whereas the Model 40 has a slew rate of only 10V/μs, but settles to 0.01% in 5μs.

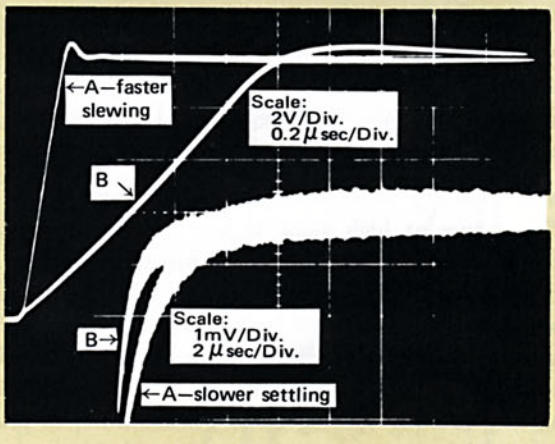


Figure 6. Comparison of Two Amplifiers Having Similar Settling Times, But Differing Slew Rates.

OTHER EFFECTS. Dielectric absorption (hysteresis), both internal to the amplifier and inherent in external bypass capacitors, may be an important factor in circuits requiring settling to 0.01%. Most capacitors used in electronic circuits have non-negligible dielectric hysteresis when used in precision applications; the popular ceramics, for example, may have typically 5%. When a capacitor is subjected to a sudden stress, it requires a period of "soaking" to return to internal charge equilibrium.[4] Thus the dC/dt term cannot be neglected in the definition of current, $i = dQ/dt = d(CV)/dt = C\,dV/dt + V\,dC/dt$. Dielectric absorption is responsible for the long "tails" (typically 10 to 100μs) often greatly extending the final-settling interval for otherwise fast amplifiers. With proper attention, an amplifier's settling time to 0.01% need not greatly be affected by dielectric

absorption, and minimization of its effects in settling to 0.1% is even less difficult to achieve.

Thermal Transients ("self-heating" effects). During slewing, the normally equal distribution of dissipations in (particularly) the input stage may become grossly unbalanced. Amplifiers designed to be fast usually run at "rich" values of current (to enable rapid handling of voltage changes across circuit capacitances and keep impedance levels down), but because a differential temperature change of one degree in a bipolar transistor stage can cause about 2 millivolts of drift (0.02% of 10-volt full scale), the time required to recover thermal balance after large input transients is a factor tending to limit the choice of currents in the input stage. In addition, a large change in load current may significantly change dissipations in the output stage (and hence temperatures inside the amplifier package), and if these temperature changes are unequally conducted to the two sides of the input stage, transient, as well as steady-state unbalances can result. Input circuit effects are less serious in inverting amplifier configurations than they are in unity-gain followers, where common-mode swing (equal to full-scale input voltage swing) may cause substantial changes in input-stage dissipation. Self-heating effects will generally not affect the settling time to 0.1%, and – in well-designed amplifiers – will not substantially increase the settling time to 0.01%. However, where this design factor is neglected, they can cause "tails" exceeding milliseconds in duration.

MINIMIZING SETTLING TIME SUGGESTIONS FOR THE CIRCUIT DESIGNER

If the designer of a typical fast-settling operational amplifier has done the job properly, taking into account all the factors we have mentioned, he has made available a device that can be demonstrated to have a specified accuracy of 0.01% and settling time less than 1μs. However, an operational amplifier is a building block in a circuit that also has a feedback network, input connections, power supply connections, output connections, and a number of external components. What has been painstakingly gained in amplifier design can be lost in short order through careless circuit design. Some of the elements of good design are these:

CONNECTIONS. It is of utmost importance that the power supply leads be adequately bypassed directly at the amplifier's terminals* and that especial care be taken in the signal and power ground circuits to avoid inducing or generating extraneous voltages in the ground signal paths.[5]

COMPONENTS. Resistors are preferably metal film types, because they have less capacitance and stray inductance than wirewound types, and are now available with excellent accuracies and temperature coefficients.

Diodes are hot carrier types for the very fastest-settling applications, but 1N914 types are suitable for more routine uses.

Capacitors in critical locations are polystyrene, teflon, or polycarbonate, to minimize dielectric absorption.

CIRCUIT. For the fastest settling times, keep leads short, orient components to minimize stray capacitance, keep circuit impedance levels as low as consistent with the output capabilities of the amplifier and the signal source, reduce all external load capacitances to the absolute minimum. Don't overlook sockets or printed circuit board mounting as possible sources of dielectric absorption. Avoid pole-zero mismatches in the feedback networks used with the amplifier. Minimize noise pickup.

*Most well-designed discrete op amps have bypass capacitors built in, but the designer should never take it for granted that they will be adequate for his application, until he can so demonstrate.

SPECIFYING SETTLING TIME

On page 2 is a statement relating to alternate definitions of settling time employed in some portions of the industry. When it comes to *specifying* settling time, there are as many formats as there are manufacturers. Until the format to be discussed and demonstrated below was developed, no known manufacturer, including Analog Devices, had presented, as a settling time specification, much more than the stark statement: "settling time as an inverter to 0.01% of full scale is . . . .μs," plus a waveform or two, and a simplified schematic of a test setup.

Important unanswered questions were: "What are the tradeoffs?" How much can settling time be reduced by reducing full-scale signal level (and thus the slewing and recovery periods)? Suppose one does not desire 0.01% accuracy, but wishes instead to determine the size of error band for a given step size and settling time? Is settling time symmetrical for positive and negative excursions?

V CURVES (Figure 7)

A graphical form of specification has been developed that helps answer many of the above questions. Because of the shape of the curves when plotted linearly, they have been dubbed "V Curves." For increased information content, however, a semilog plot has been adopted. Each curve represents the measured settling time (microseconds) vs full-scale step magnitude (volts) for a given final error band. Three error bands were chosen: ±1mV, ±10mV, ±100mV, corresponding to ±0.01%, ±0.1%, ±1% of full scale, respectively. The percentage error is the ratio of error band to output step. For example, 1mV/5V = 0.02%.

Information is given for both positive and negative step polarities; the two standard configurations shown are as unity gain inverter and unity gain follower. It is of course possible to obtain data for curves for other conditions, and we welcome comments by our readers on the adequacy and relevance of this form of specification, along with suggestions for improvements to the format.

Figure 7 shows a set of theoretical V Curves for an ideal amplifier having no slew rate difficulties whose τ_x is 100ns

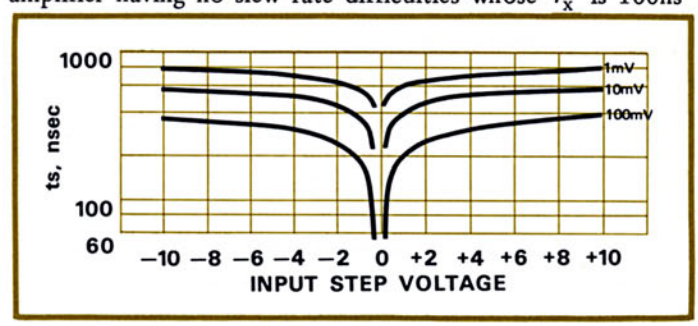


Figure 7. Example of V Curves. Theoretical Amplifier With First-Order Linear Response.

(f_x = 1.6MHz). Figure 8 shows the curves, accompanied by photographs of typical oscilloscope traces, for AD Model 45, a FET-input amplifier capable of settling to within ±0.01% of full scale in less than 1μs.

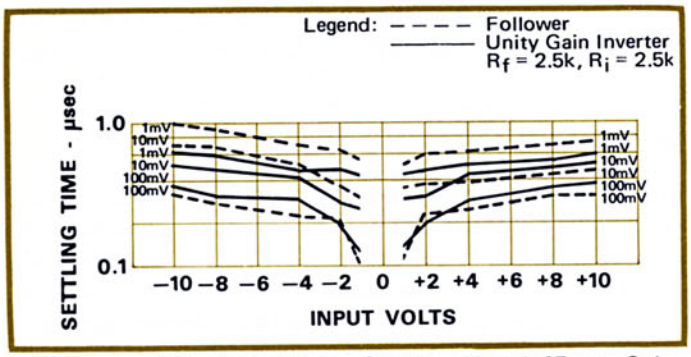


Figure 8. Example of V Curves. Model 45: a Sub-microsecond-settling FET-Input Economy Op Amp.

AMPLIFIER V-CURVES

In Figure 9 are shown V Curves for an assortment of amplifiers. Although it is evident that only a few of these types have been specifically optimized for settling time,

1. a number of them settle quickly enough to be used for a variety of less critical applications

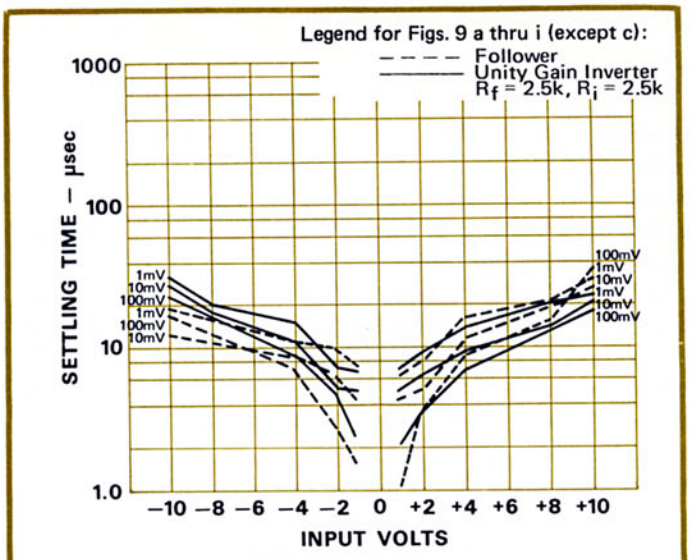
2. others among them are general-purpose types for which detailed settling time data have simply never been available. Their wide usage and low cost make such data particularly useful.

Further, in order to assist the reader in obtaining perspective on relative amplifier behavior within the industry by a consistent set of measurements, we have included data from our measurements on several amplifier types which, though not available from Analog Devices, may be of interest to our readers. Included are:

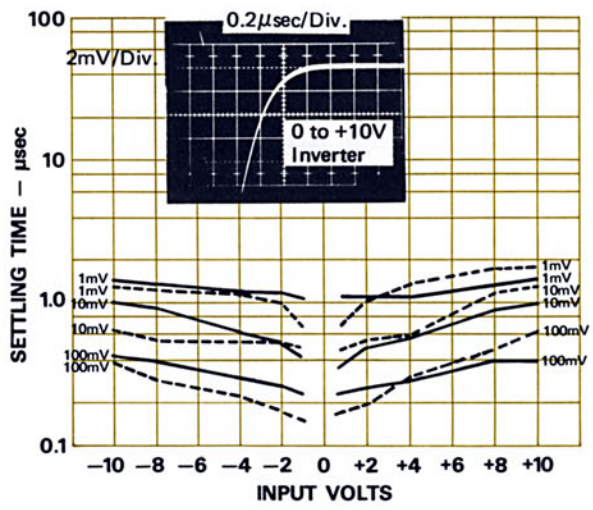
Fig.9a Model 40, a low-cost general-purpose FET-input type
Fig.9b Model 149, a high-slew rate FET-input type
Fig.9c Model 120, a bipolar-input fast feed-forward type (inverting only)
Fig.9d Model 180, a low-drift bipolar type
Fig.9e Model AD741, a bipolar-input general-purpose IC type
Fig.9f Model AD503, a FET-input IC-type with 741 output stage (but increased speed!)
Fig.9g Model μA715, a fast-settling IC type, using recommended stabilization (Fairchild Semiconductor)
Fig.9h Model 1011, a FET-input medium fast amplifier (Teledyne Philbrick/Nexus)
Fig.9i Model 3308, a low-cost general-purpose FET-input type (Burr-Brown)

The measurements which resulted in these curves were by and large made during the summer and fall of 1969, and so may not include amplifiers that approach the state of the art today. In addition to the curves published here for the representative selection of types, a considerable amount of data has been taken on a wide variety of other amplifier types in our product line. We will be pleased to respond to inquiries regarding specific types for which information may be available.

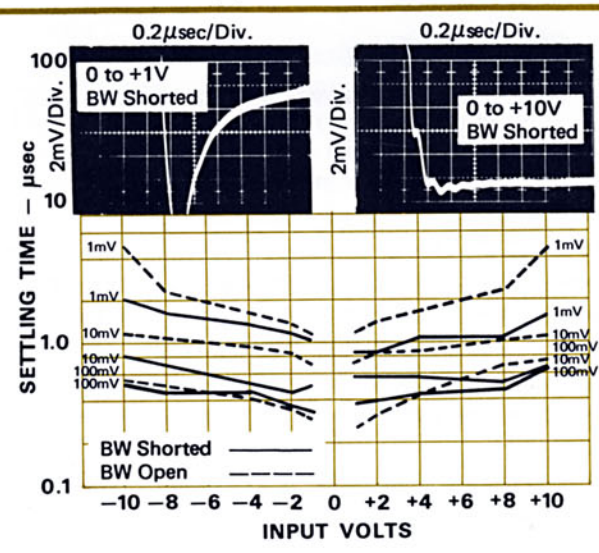
Figure 9. Amplifier V Curves and Typical Responses. →



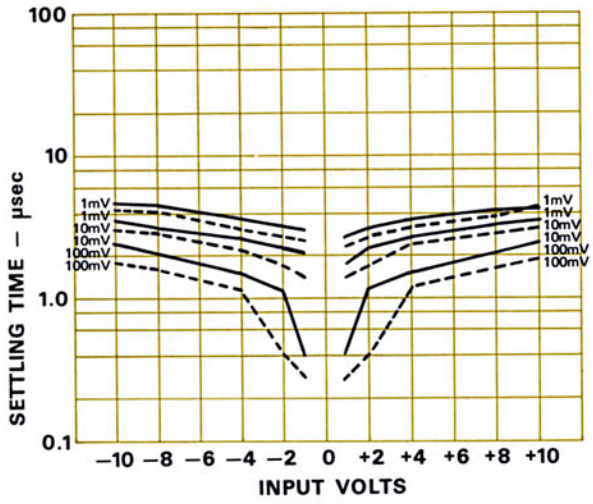
(a) Model 40



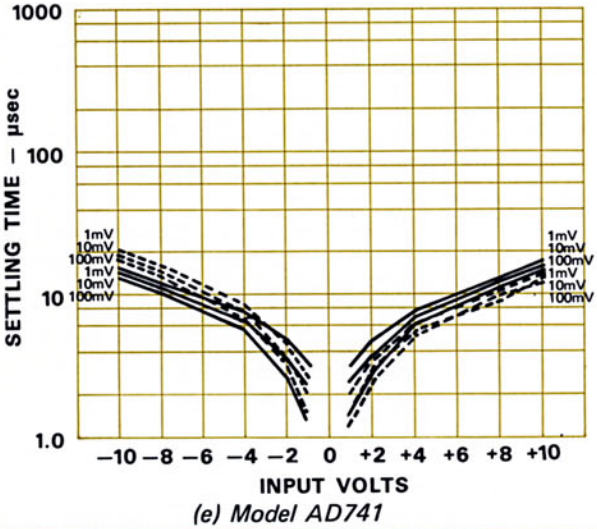
(b) Model 149



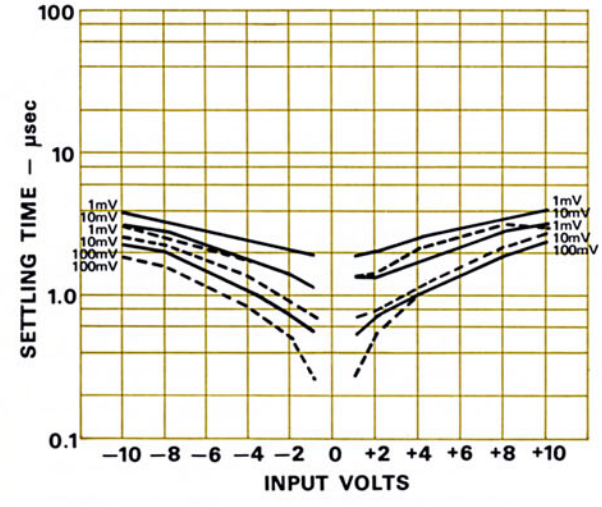
(c) Model 120 (BW Shorted and BW Open)



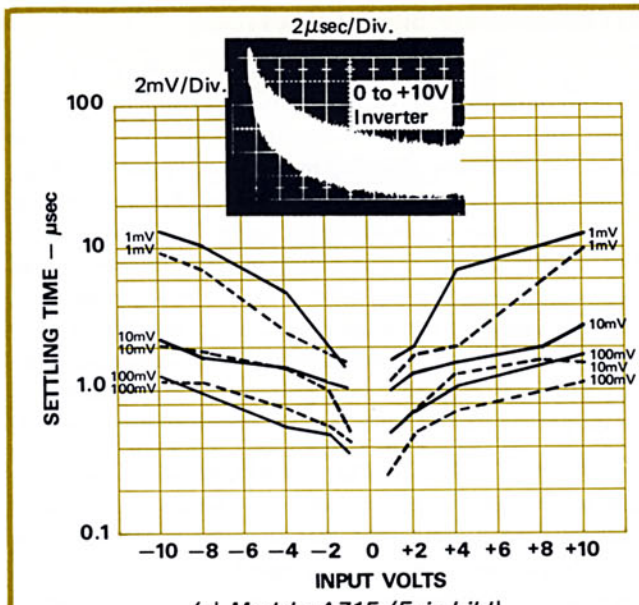
(d) Model 180



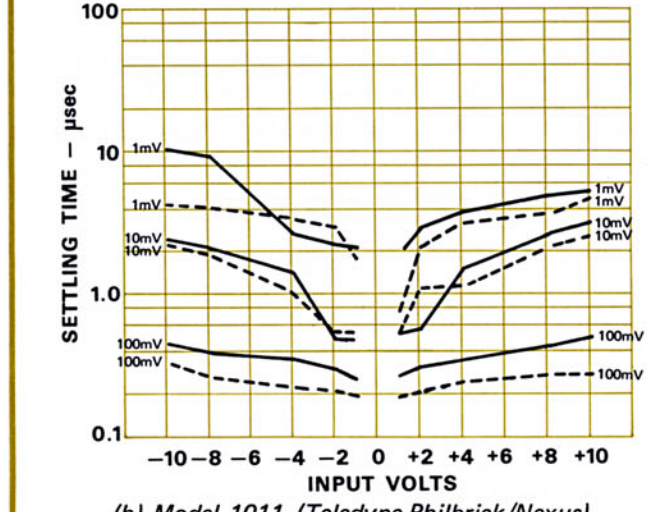
(e) Model AD741



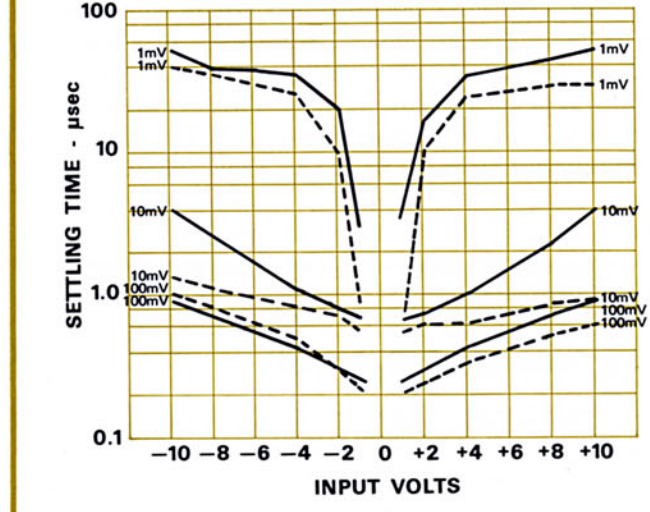
(f) Model AD503



(g) Model µA715 (Fairchild)



(h) Model 1011 (Teledyne Philbrick/Nexus)



(i) Model 3308 (Burr-Brown)

LIMITATIONS OF SPECIFICATIONS

CIRCUITS STUDIED. It is usually the case that for most operational amplifiers, the fastest-settling performance will be obtained when the amplifier is operated as either a unity-gain inverter or as a follower. (*Slewing* may be more rapid, however, for some types, at high closed-loop gains). For this reason, data has been taken at unity gain using both inverter and follower configurations. The amplifiers operate with no external resistive or capacitive load, other than the comparator used for the measurement, the leads to it, and the feedback circuit impedance in the inverting configuration. The resistance component has been confined to a pair of 2.5kΩ resistors, to enable amplifiers having 5mA output current to be measured.

EXTRAPOLATION OF SETTLING TIME MEASUREMENTS. Because of the many factors that influence settling time, it may be dangerous to assume that data may be interpolated (or worse, extrapolated), especially for those types having radical changes in shape between adjacent curves, or in different portions of the same curve.

AMPLIFIER STABILIZATION NETWORKS. The methods used for feedback stabilization can have quite drastic effects on the amplifier's settling time because the amplifier's settling characteristics are intimately related to the location of both the open loop and closed loop poles and zeros. Anything the user does that will reduce the amplifier's bandwidth will usually lengthen settling time. For example, multiple input summing resistors decrease loop gain; added summing point capacitance requires feedback capacitance to compensate, resulting in smoother (but often slower) settling; output cable capacitance can cause peaking, and may require a load isolation resistor, which will result in slower overall response; stray feedback capacitance. Even such a simple thing as placing a resistive load on the amplifier may reduce its open-loop gain (at all frequencies, including f_X), and thus its loop gain and settling time.

CAVEAT. Since settling time specifications cannot possibly include (or be extrapolated to) all possible situations, they should be used as a guide for preliminary selection of an amplifier to fit a given application. In all cases, and especially where the application conditions are significantly different from those used in specifying the amplifier, there can be no substitute for actual trial of the amplifier in the proposed circuit to determine whether it will perform as desired. Often, the manufacturer's experience with customers having a wide variety of applications can be helpful, and – especially where op amps are key elements in large important projects – designers are urged to make use of the manufacturer's applications engineers for helpful suggestions and judgements based on their experience.

MEASURING SETTLING TIME

INVERTING CONFIGURATION

There are a number of circuit approaches that may be used for observing the settling time of an inverting amplifier. Perhaps the simplest (or at least the most obvious) consists of measuring the voltage at the amplifier's own error point. Though superficially simple, this method has several deficiencies: the added capacitance of the measuring device affects the closed-loop dynamics, the dynamic input impedance of the amplifier may cause errors in estimating the actual gain error, and feedback circuit dynamics may introduce errors that will not be observable at the error point.

Instead of using the actual summing point of the amplifier, it is feasible to construct a quasi-summing point, as shown in Figure 10. Although measurement errors may be caused by capacitance at this quasi-summing point, it does not affect amplifier performance. Because the comparator which observes the error is comparing the proxy error signal with "ground," this is by far the easiest kind of measurement to make. The comparator's output is readily clamped to minimize overdrive of both the comparator and the monitoring oscilloscope, the comparator may have gain, and it may also settle more slowly than the amplifier under test (its settling time errors are second-order, in this case.)

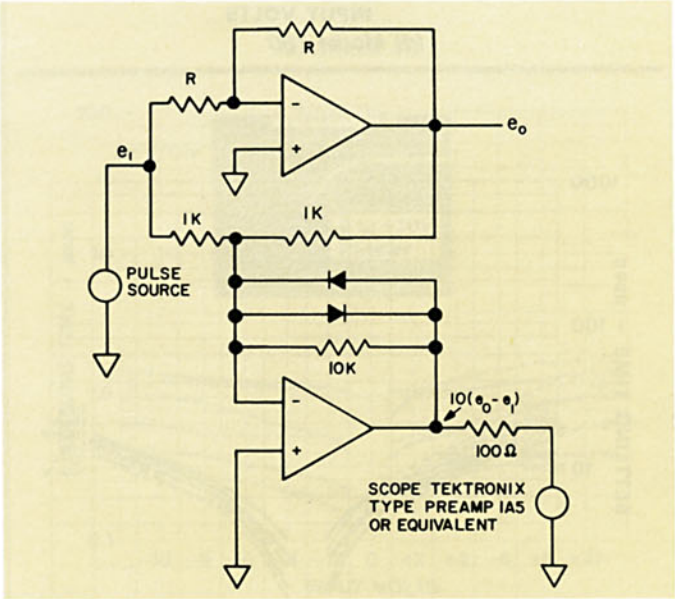


Figure 10. Settling Time Measurements at Quasi-Summing Point.

The above discussion pertains to an amplifier used with a voltage signal and input and feedback resistors. However, if the signal is a current step (amplifier used as a current-to-voltage transducer), the output step response must be compared with the expected final value. Since the comparator is taking the difference directly, rather than observing an error point, it will be subjected to wider swings, and it must settle substantially (at least 2 to 3 times) faster than the amplifier under test to avoid introducing excessive delay and time uncertainty. Needless to

IN THE NEXT ISSUE

Prediction can be dangerous in this game (as witness our prediction of four Dialogue issues in 1969, which turned out to be 25% accurate). However, for the next issue we are planning to publish two sorely-needed items:

1. A new approach to describing the performance of and specifying analog multipliers.

2. A comparative evaluation of today's electrometers, including parametrics, MOS-FET's, and some suggestions for getting the most out of parametrics in the area of femtoamp (i.e., 10^{-15} amp) resolution levels.

say (having already dwelt heavily on the problems of designing a fast-settling amplifier itself), the problem of designing and instrumenting a comparator to test settling time (and properly interpreting the results obtained with it) presents challenges that make the amplifier design job look easy.

NON-INVERTING CONFIGURATION. The most usual circuit to be tested is the unity-gain follower. It requires direct comparison between the input step and the output signal as they swing through the entire common-mode range. Thus the problem, and its instrumentation, may be similar to that of the inverter with current source.

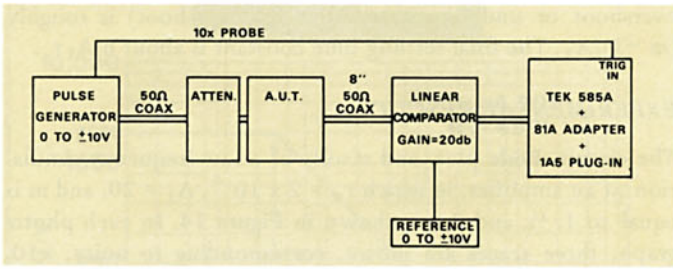


Figure 11. Instrumentation for Settling Time Measurement

EQUIPMENT. Figure 11 shows a typical measurement system for settling time. Commercially available comparators, such as the Tektronix Models W and 1A5, the Hewlett-Packard 1803A, and the Adage Ultranull NDI are useful, but their applicability is limited to settling times somewhat greater than 1μs for 0.01% measurements. As a rule, specially-designed and constructed equipment is required in order to assure oneself that the system requirements are met, including low noise, minimization of excess lead inductance, capacitance, and (naturally) adequate settling time.

The pulse generator used for the measurement should have rise times of the order of 10ns, with a flat top occurring within (say) a few hundred nanoseconds of the step transition. A square wave of about 100Hz should be applied initially to determine output amplitude and whether the amplifier exhibits slow recovery phenomena (due to thermal transients, dielectric absorption, etc.) Once the observer is satisfied of the absence of long tails, a much faster rate may be used to observe fine structure. Some low cost signal generators exhibit a degree of pulse "droop," that may cause what appear to be long tails in observations of settling time of an amplifier, especially in the follower configuration (because the amplifier output is being compared with a dc level). The dummy summing point approach of Figure 10 is less sensitive to pulse droop, because addition of input and output waveforms tends to cancel the droop, assuming that the amplifier reproduces the droop with fidelity.

Most of the measurements performed to obtain the V curves used the specially-constructed square wave source and comparator schematically illustrated in Figures 12 and 13. The square wave source is capable of supplying both positive and negative outputs variable from zero to ±10 volts, with a rise time of about 15 nanoseconds.

The comparator shown was used for all but the fastest amplifiers. It settled in about 0.75μs for measurements in a 1mV error band, and about 0.5μs for measurements in the 10mV error band. Its performance had been intentionally compromised by adjusting its input impedance so that it could be used for measuring outputs of G.P. amplifiers having only 5mA available. (Amplifiers designed for fast settling usually have outputs of 20mA or more).

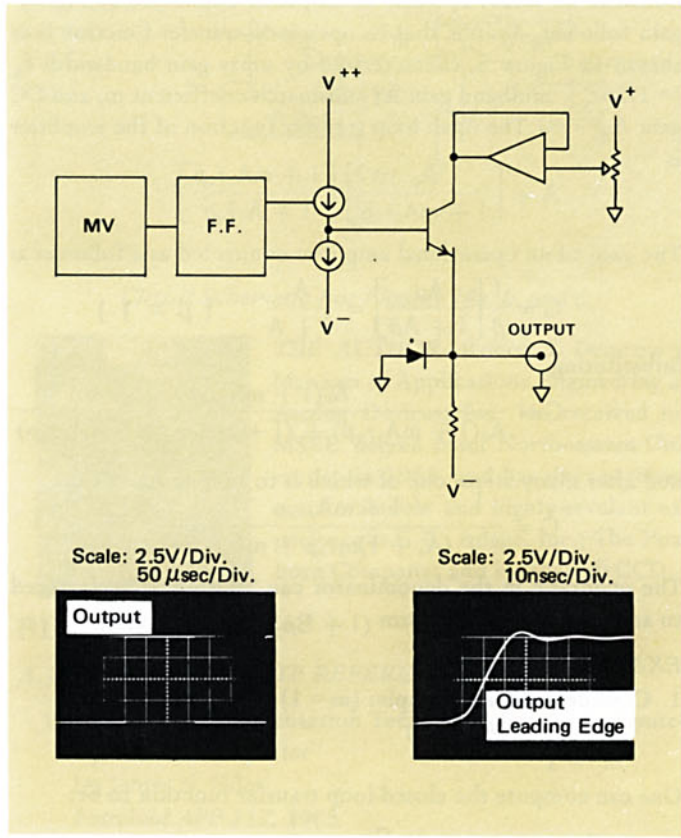


Figure 12. Square Wave Source, Simplified.

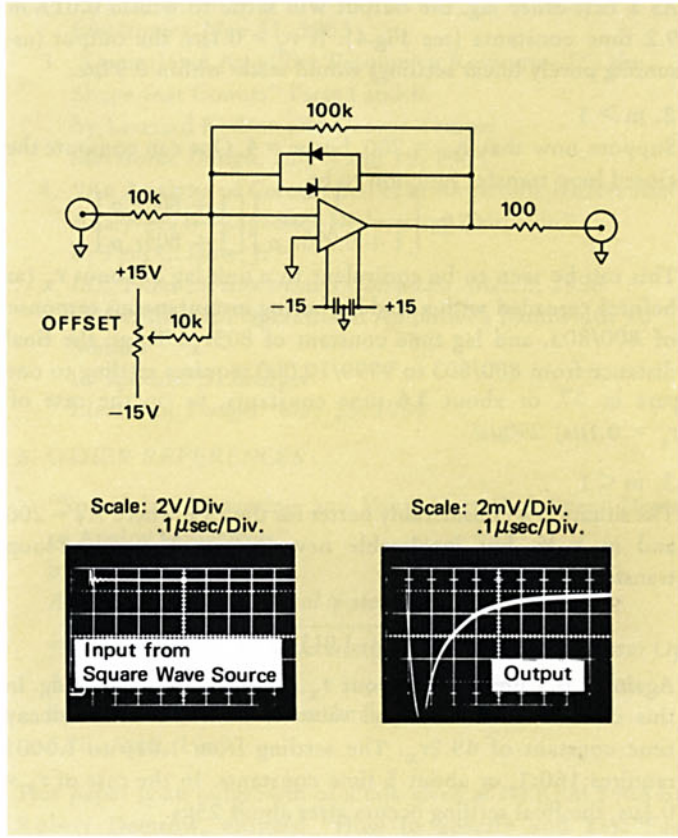


Figure 13. Comparator Simplified

APPENDIX

EFFECTS OF POLE-ZERO MISMATCH ON LINEAR-SETTLING INTERVAL

Consider an ideal* operational amplifier connected as a unity-gain follower. Assume that its open-loop transfer function is as shown in Figure 5, characterized by unity-gain bandwidth f_x ($= 1/2\pi\tau_x$), midband gain A_1, mismatch coefficient m, and DC gain $A_0(\rightarrow \infty)$. The open loop transfer function of the amplifier is

$$A = \left[\frac{A_0}{1 + mA_0\tau_x p}\right]\left[\frac{1 + mA_1\tau_x p}{1 + A_1\tau_x p}\right]$$

The gain of an operational amplifier connected as a follower is

$$G = \frac{1}{\beta}\left[\frac{A\beta}{1 + A\beta}\right] = \frac{A}{1 + A} \qquad (\beta = 1)$$

Substituting,

$$G = \frac{A_0(1 + mA_1\tau_x p)}{A_0(1 + mA_1\tau_x p) + (1 + mA_0\tau_x p)(1 + A_1\tau_x p)}$$

and after many steps, one of which is to assume $A_0 \rightarrow \infty$,

$$G = \frac{1 + mA_1\tau_x p}{1 + (A_1 + 1)m\tau_x p + mA_1\tau_x^2 p^2}$$

The quadratic in the denominator can, of course, be factored to an expression of the form $(1 + Bp)(1 + Cp)$

EXAMPLES

1. Consider now an example: (m = 1)

$A_1 = 200$ $(A_0 \rightarrow \infty)$

$m = 1$

One can compute the closed-loop transfer function to be:

$$G = \frac{1}{1 + \tau_x p}$$

As a first-order lag, the output will settle to within 0.01% in 9.2 time constants (see Fig.4). If $\tau_x = 0.1\mu s$, the output (assuming purely-linear settling) would settle within $0.92\mu s$.

2. $m > 1$

Suppose now that $A_1 = 200$, but m = 4. One can compute the closed-loop transfer function to be

$$G \cong \left[\frac{1}{1 + 0.996\tau_x p}\right]\left[\frac{1 + 800\tau_x p}{1 + 803\tau_x p}\right]$$

This can be seen to be equivalent to a unit-lag of about τ_x (as before) cascaded with a lead-lag having instantaneous response of 800/803, and lag time constant of $803\tau_x$! To go the final distance from 800/803 to 9999/10,000 requires settling to one part in 37, or about 3.6 time constants, or (in the case of $\tau_x = 0.1\mu s$) $290\mu s$!

3. $m < 1$

The situation is considerably better for the case where $A_1 = 200$ and m = ¼, but intolerable nevertheless. The closed-loop transfer function is

$$G \cong \left[\frac{1}{1 + 1.015\tau_x p}\right]\left[\frac{1 + 50\tau_x p}{1 + 49.2\tau_x p}\right]$$

Again, it is a unit lag of about τ_x, cascaded with a lead-lag. In this case, there is an initial value of 50/49.2, with a decay time constant of $49.2\tau_x$. The settling from 1.016 to 1.0001 requires 160:1, or about 5 time constants. In the case of $\tau_x = 0.1\mu s$, the final settling occurs after about $25\mu s$.

*"Ideal" in terms of input and output impedances, CMRR, and every other respect, except gain and frequency response.

In the above examples, neglecting the initial fast settling interval accounted for a conservative 7 time constants (i.e., for settling to well within 0.1%), or about $0.7\mu s$.

APPROXIMATION

A reasonable approximation for pole-zero mismatch response calculations, especially for m closer to unity than in the exaggerated example above, is to assume that the amplifier settles to within $1/A_1$ initially in exponential manner, with time constant τ_x. The number of time constants can be estimated quickly from the table in figure 4. The amount of overshoot or undershoot (positive for overshoot) is roughly $(m - 1)/A_1$. The final settling time constant is about $mA_1\tau_x$.

EXPERIMENTAL RESULTS

The circuit, Bode plot, and results of a low-frequency simulation of an amplifier, in which $\tau_x = 2 \times 10^{-4}$, $A_1 = 20$, and m is equal to 1, ½, and 2, are shown in Figure 14. In each photograph, three traces are shown, corresponding to unity, x10, and x100 magnification of the error band (i.e., the final settling interval). In this example, the amplifier simulated was connected as a unity-gain inverter. The reason the simulation was performed at low frequency was to retain as complete as possible control over the idealized characteristic, eliminating slewing phenomena, dielectric absorption, etc.

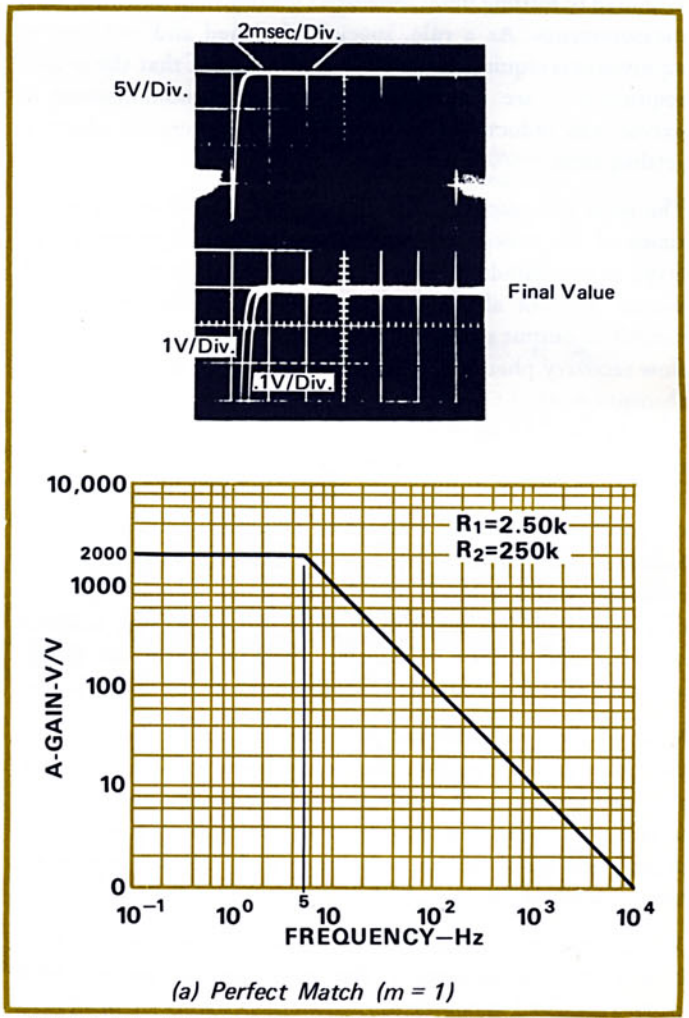
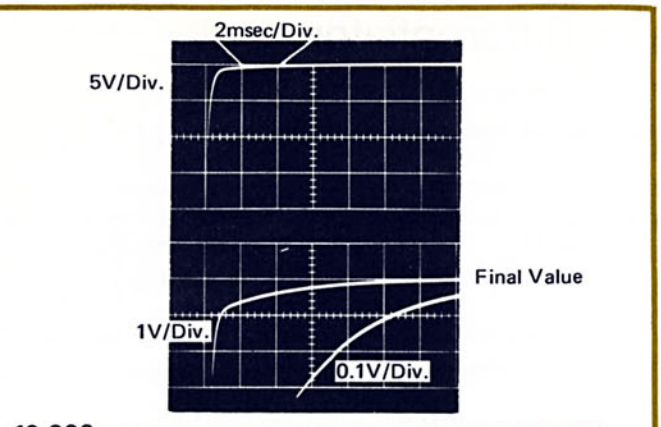
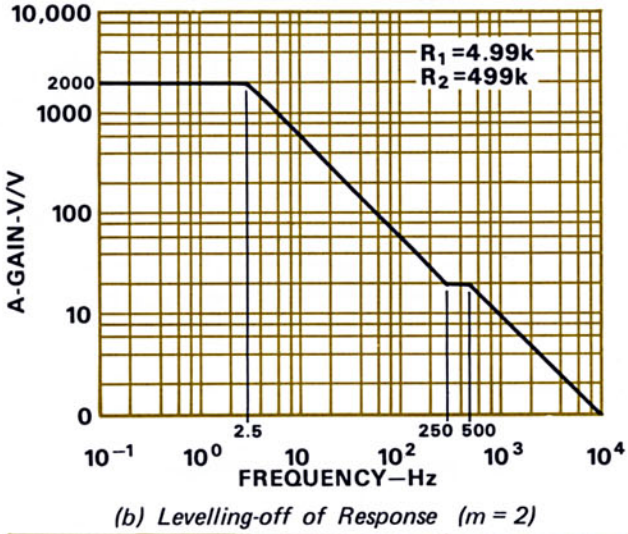
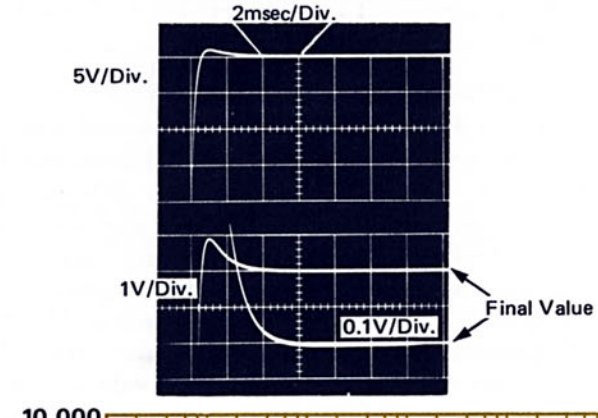


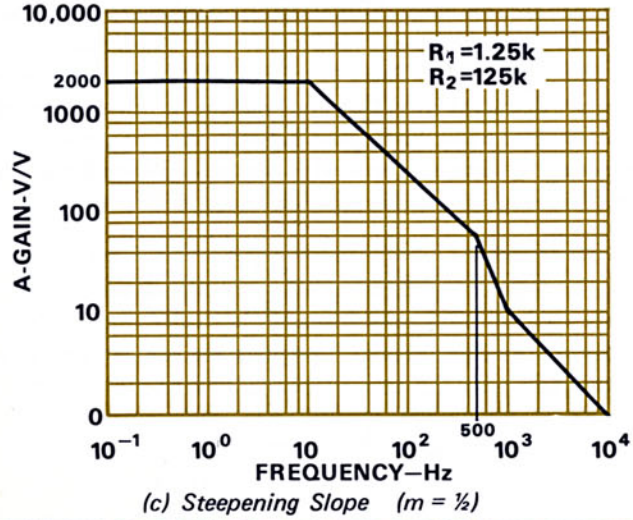
Figure 14. Small-Signal Settling as a Function of Pole–Zero Match (Low Frequency Model)



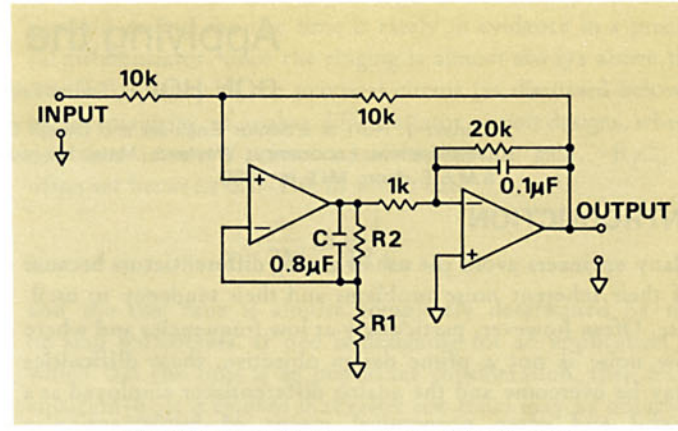


(b) Levelling-off of Response (m = 2)





(c) Steepening Slope (m = ½)



Circuit Schematic For Figures 14a, b, and c.

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EEE. April, 1969

This paper is an outgrowth of a talk given at NEREM 1968 by Robert Demrow, entitled "How to Specify and Test Fast Settling Operational Amplifiers."

Applying the Analog Differentiator

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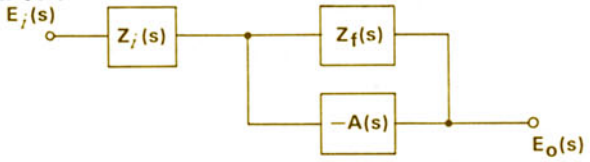
INTRODUCTION

Many engineers avoid the use of analog differentiators because of their inherent noise problems and their tendency to oscillate. Often however, particularly at low frequencies and where low noise is not a prime design objective, these difficulties may be overcome and the analog differentiator employed as a useful and often economical means of implementing a circuit requirement.

This paper analyzes the basic analog differentiator operation and discusses the limitations imposed by finite operational amplifier gain and bandwidth. Means for minimizing instabilities and noise at high frequencies are discussed as well as the requirements for obtaining improved rise time performance.

ANALYSIS

The basic circuit configuration for a feedback amplifier is shown below



The closed loop gain of this circuit is given by*

$$\frac{E_o(s)}{E_i(s)} = -\frac{Z_f(s)}{Z_i(s)}\left[\frac{1}{1+\frac{1}{A(s)\beta(s)}}\right]$$

If the gain, A, is very high, then $A(s)\beta(s) \gg 1$, and the closed loop gain is very nearly equal to

$$\frac{E_o(s)}{E_i(s)} \cong -\frac{Z_f(s)}{Z_i(s)}$$

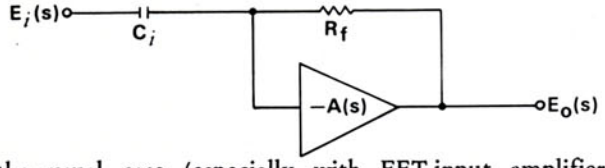
For the general case, however,

$$\beta(s) = \frac{Z'(s)}{Z'(s)+Z_f(s)}$$

Where $Z'(s)$ is the parallel combination of $Z_i(s)$ and R_d, the input impedance (in this case assumed resistive) of the amplifier. Then

$$\frac{E_o(s)}{E_i(s)} = -\frac{Z_f(s)}{Z_i(s)}\left[\frac{1}{1+\frac{1}{A(s)}\left(1+\frac{Z_f(s)}{Z'(s)}\right)}\right]$$

For a differentiator, $Z_f(s)$ is a resistor R_f, and $Z_i(s)$ becomes a capacitive reactance.



In the usual case (especially with FET-input amplifiers) $R_d \gg X_{C_i}$, therefore

$$Z'(s) = \frac{R_d\left(\frac{1}{sC_i}\right)}{R_d+\frac{1}{sC_i}} \cong \frac{1}{sC_i} = Z_i(s)$$

*"Operational Amplifiers, Part 1," Analog Devices, Inc., Applications Manual.

and

$$\frac{E_o(s)}{E_i(s)} = -sR_fC_i\left[\frac{1}{1+\frac{1}{A(s)}(1+sR_fC_i)}\right]$$

For an operational amplifier, the gain as a function of frequency is given by

$$A(s) = \frac{A_0}{1+T_0 s}$$

where A_0 is the low frequency gain, $1/T_0$ is the (radian) frequency breakpoint, and $\omega_c = A_0/T_0$ is the unity gain frequency (Figure 1).

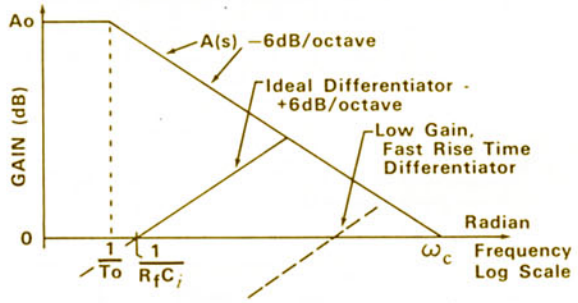


Figure 1. Bode Plot of Ideal Differentiators

Then (1)

$$\frac{E_o(s)}{E_i(s)} = \underbrace{-sR_fC_i}_{\text{IDEAL DIFFERENTIATOR}}\underbrace{\left[\frac{1}{1+\left(\frac{1+T_0 s}{A_0}\right)(1+sR_fC_i)}\right]}_{\text{ERROR TERMS}}$$

The first term is the ideal response, while the second term, in brackets, is the error caused by finite gain and bandwidth. If the gain, $A_0 \to \infty$, then we have the ideal differentiator characteristic (gain increasing with frequency) shown plotted in Figure 1. Typically the operating frequency range of a differentiator is around the frequency at which the gain is 0dB. From the figure, it is apparent that (1) highest gain is obtained at high frequencies, thus making the differentiator susceptible to high frequency noise and, (2) an unstable condition is produced because the ideal differentiator function (+6dB/octave) closes on the gain curve (−6dB/octave) at 12dB/octave (i.e. with 180° phase shift). These problems, which are readily overcome, are discussed later. However, valuable insights into a differentiator's extreme high speed behavior may be obtained by computing its time response with the idealized feedback network. Rearranging equation (1) while noting that $1/A_0 \cong 0$, gives

$$\frac{E_o(s)}{E_i(s)} = -s\omega_c\left[\frac{1}{s^2+s\left(\frac{1}{R_fC_i}+\frac{1}{T_0}\right)+\frac{\omega_c}{R_fC_i}}\right]$$

We are now in a position to "complete the square" to obtain the Laplace Transform in the "standard" form

$$\frac{1}{(s+a)^2+b^2}$$

This operation yields (2) $\frac{E_0(s)}{E_i(s)} =$

$$-s\omega_c\left[\frac{1}{\left(s+\left[\frac{1}{2T_0}+\frac{1}{2R_fC_i}\right]\right)^2+\left(\frac{\omega_c}{R_fC_i}-\left[\frac{1}{2T_0}+\frac{1}{2R_fC_i}\right]^2\right)}\right]$$

Before proceeding to obtain the inverse transform of this equation, we find that, for typical values of parameters in operational amplifier differentiators,

$$(3)\qquad \frac{\omega_c}{R_fC_i} \gg \left(\frac{1}{2T_0}+\frac{1}{2R_fC_i}\right)^2$$

With this simplification, equation (2) becomes

$$(4)\qquad \frac{E_0(s)}{E_i(s)} \cong -s\omega_c\left[\frac{1}{\left(s+\left[\frac{1}{2T_0}+\frac{1}{2R_fC_i}\right]\right)^2+\frac{\omega_c}{R_fC_i}}\right]$$

This is the £-transform equation of the basic analog differentiator, taking into account the amplifier's open-loop gain characteristic.

RAMP INPUT

To illustrate the performance of the differentiator, consider the response of (4) to a linear ramp input (i.e., a signal whose derivative steps from zero at the beginning of the ramp to a constant value, k)

$$e_i(t) = kt \qquad (k = \text{constant})$$

$$(5)\quad \text{or} \qquad E_i(s) = \frac{k}{s^2}$$

Equation (4) then becomes

$$E_0(s) = -\frac{k\omega_c}{s}\left[\frac{1}{\left(s+\left[\frac{1}{2T_0}+\frac{1}{2R_fC_i}\right]\right)^2+\frac{\omega_c}{R_fC_i}}\right]$$

Taking the inverse transform yields

$$e_0(t) = -\frac{k\omega_c}{(\omega_c/R_fC_i)^{1/2}}\int_0^t e^{-\left(\frac{\omega_c}{2A_0}+\frac{1}{2R_fC_i}\right)t}\sin\left(\frac{\omega_c}{R_fC_i}\right)^{1/2} t\,dt$$

Performing the integration and noting the inequality (equation 3) yields the output given by (6) and depicted in Figure 2.

$$(6)\qquad e_0(t) = kR_fC_i\left[e^{-\left(\frac{\omega_c}{2A_0}+\frac{1}{2R_fC_i}\right)t}\cos\left(\frac{\omega_c}{R_fC_i}\right)^{1/2} t - 1\right]$$

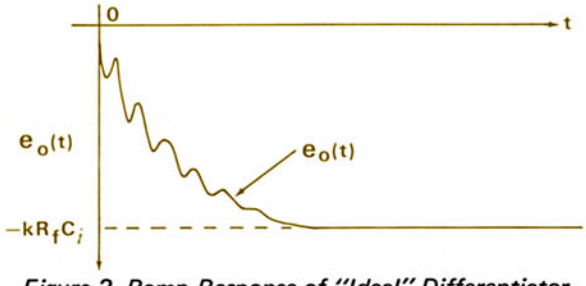


Figure 2. Ramp Response of "Ideal" Differentiator

Considerable insight into differentiator performance may be obtained from equation (6) and Figure 2 for the basic circuit. As expected, the differentiator output response to a linear ramp is seen to be a DC level proportional to the magnitude, k, of the input ramp. The gain of the circuit is equal to $-R_fC_i$, while the rise time is a function of the operational amplifier parameters (ω_c and A_0) as well as the external circuit elements (R_f and C_i). The superimposed damped sinusoid during the rise time is rarely in evidence in a practical differentiator, since the ringing is almost always above the cutoff frequency of the practical circuit (as discussed below). In the majority of analog differentiator circuit designs, where rise time is not a prime consideration, the gain, $-R_fC_i$, is often set between 0.1–1.0, in which case

$$\frac{\omega_c}{2A_0} \gg \frac{1}{2R_fC_i}$$

and the rise time is almost completely determined by the op amp parameters. If one is designing for an application in which fast rise time is an important consideration, then, from equation (6), it is evident that faster rise times may be obtained by selecting R_f and C_i, (shown in Figure 1) as small as possible. This improvement in τ_r is obtained, however, at the expense of circuit gain (gain = $-R_fC_i$), which may, of course be recouped by following the differentiator with a wideband amplifier. (The small output amplitude will also have less tendency to tax the slew rate capability of the amplifier.)

If the differentiator is being utilized to measure the slope of the input ramp, the accuracy of measurement at a time t_1 is seen to be very nearly

$$\text{Accuracy } (\%) \cong 100\, e^{-\left(\frac{\omega_c}{2A_0}+\frac{1}{2R_fC_i}\right)t_1}$$

PRACTICAL CONSIDERATIONS

Earlier it was pointed out the basic analog differentiator is susceptible to high-frequency noise amplification and instabilities (due to capacitance to ground at the input and output of the amplifier in practical circuits, and to greater than 6dB/octave rolloff slope in many available amplifiers). A common technique utilized to improve circuit performance with respect to both problems is the addition of a single or double 6dB/octave "breakpoint," as shown in Figures 3 and 4.

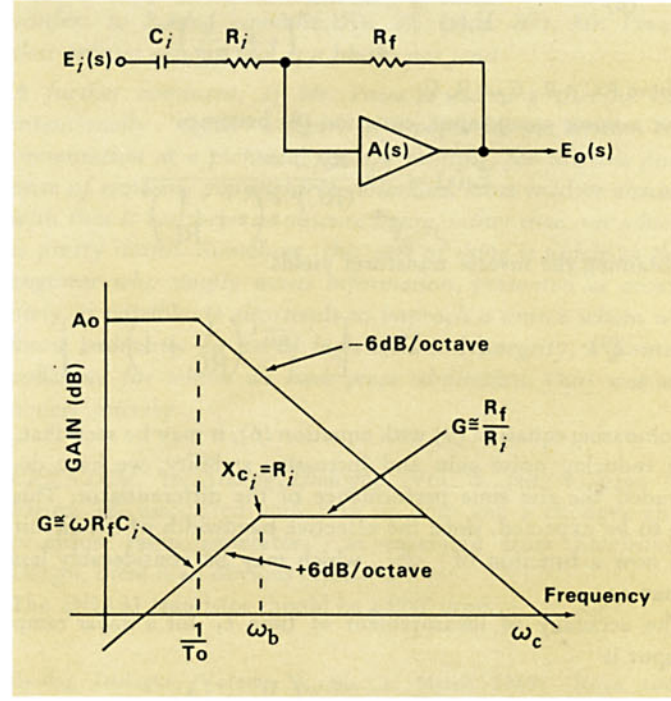


Figure 3. Bode Plot of Differentiator with First-order Rolloff

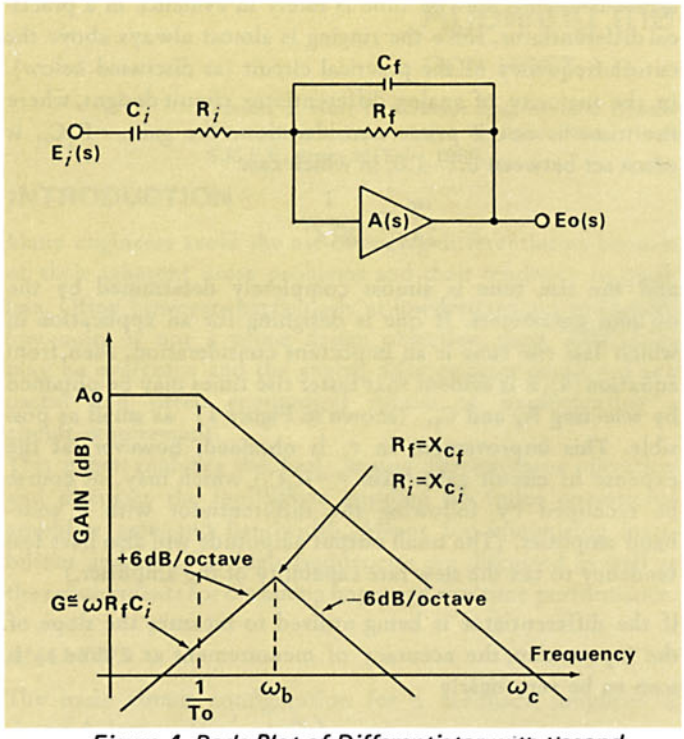


Figure 4. Bode Plot of Differentiator with Second-order Overdamped Rolloff

In either case, the supplementary breakpoints should be placed well enough above the maximum operating frequency to assure the required accuracy.

The expression for the transfer fraction of the circuit of Figure 4 is approximately

$$(7) \qquad \frac{E_0(s)}{E_i(s)} \cong -\frac{sR_fC_i}{(1+sR_iC_i)(1+sR_fC_f)}$$

If $R_f = X_{C_f}$ and $R_i = X_{C_i}$ at ω_b, equation (7) becomes

$$(8) \qquad \frac{E_0(s)}{E_i(s)} = -\frac{R_fC_i}{(RC)^2}\frac{s}{\left(s+\frac{1}{RC}\right)^2}$$

where $RC = R_f C_f = R_i C_i$

For a linear ramp input, equation (8) becomes

$$E_0(s) = -k\frac{R_fC_i}{(RC)^2}\frac{1}{s\left(s+\frac{1}{RC}\right)^2}$$

Obtaining the inverse transform yields

$$(9) \qquad e_0(t) = kR_fC_i\left[e^{-\frac{1}{RC}t}\left(\frac{t}{RC}+1\right)-1\right]$$

Comparing equation (9) with equation (6), it may be seen that, in reducing noise gain and increasing stability, we have degraded the rise time performance of the differentiator. This is to be expected, since the effective bandwidth of the circuit is now a function of $\frac{1}{RC}$, which may be considerably less than ω_c.

The accuracy of measurement at time t_1 for a linear ramp input is

$$\text{Accuracy} \cong 100\, e^{-\frac{1}{RC}t_1}\left(\frac{t_1}{RC}+1\right)$$

Editor's Notes:

Your response to *Analog Dialogue* and the articles we publish continues to encourage us, and to give us the heartwarming feeling that not only is the *Dialogue* important to our business, but also that we have been charged with a responsibility for the nurture of an organism whose life now has an existence of its own.

Since the last issue, much has happened at Analog Devices, with a direct bearing on the future of *Dialogue*. What it boils down to is that although our field remains the same ("Analog Technology"), our product line is now greatly expanded, with greater depth (fine structure) in a number of areas. In future issues, one can hope to read about

- Active Filters
- New Linear Integrated Circuit Designs & Applications
- Power Amplifier Applications
- System Design Using A/D and D/A Converters
- New types of Converters Using Monolithic IC's
- Analog Multiplier Specifications & Applications

Despite a number of past long silences, we may also hope to see *Dialogue* more frequently in the future.

ANALOG UPDATE. You may have noticed, in recent months, the appearance in our mailings of what seemed a poor substitute for *Dialogue*, a one-page summary of new products called *Analog Update*. Here's what *Update* is all about:

It is the technological mission of Analog Devices to identify and produce electronic function circuits having the performance you need at prices that will enable you to use them profitably in your own circuit, instrument, and system designs, and to provide you with as much as possible in the way of useful design information and applications assistance to make their use easy. To accomplish this mission requires that we communicate news of new products (or applications of existing products) to you in a timely fashion.

In the not-too-distant past, it was easy to communicate new product applications ideas because the number of new products introduced was relatively small—and they were all operational amplifiers! However, as we've grown, the number and complexity of products has greatly increased. For example, during 1969 we introduced about 20 new products, including such diverse items as Discrete and IC Operational Amplifiers, Power Supplies for Op Amps and Logic circuits, Log Circuits, an analog circuit "Solderless Breadboard," Instrumentation Amplifiers, Active Filters, etc.

To fulfill the need to communicate new product information frequently, we have initiated *Analog Update* to serve "between the *Dialogues*" as a rapid-access medium to inform you of new Analog Devices products. *Update* will continue to be brief and to the point, it will usually be accompanied by product data sheets, or other timely material, and it will appear aperiodically (but frequently!).

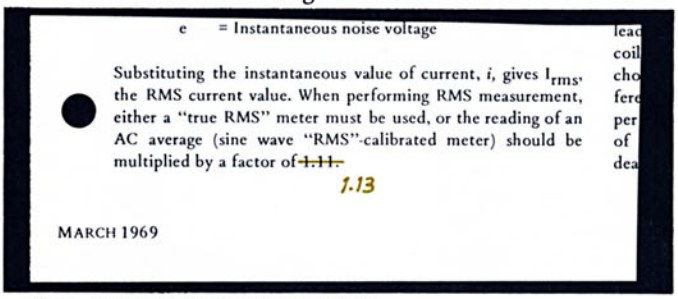
DAN SHEINGOLD

Readers' Notes:

A great many readers took the trouble to pass on a few kind words of appreciation for Dialogue. *These all said about the same thing, in many ways, and though they made fascinating reading (for us), it would serve no useful purpose to include them here. On the other hand, there were a couple that were unusually interesting, in that they discussed a point that was glossed over (and was further distinguished by a slide rule error).*

Your recent issue of *Analog Dialogue* concerning noise in operational amplifier circuits[1] was of great interest. It was an excellent discussion of noise in general and its measurement. I appreciated the differentiation between the various types of noise.

Since Hewlett-Packard's voltmeters are often used for noise measurements, I was particularly interested in your comments on page 7 regarding the characterization of noise. You mentioned that the indication on an average-responding RMS-calibrated meter should be multiplied by 1.11 to obtain the RMS value of the noise being measured.



e = Instantaneous noise voltage

Substituting the instantaneous value of current, *i*, gives I_{rms}, the RMS current value. When performing RMS measurement, either a "true RMS" meter must be used, or the reading of an AC average (sine wave "RMS"-calibrated meter) should be multiplied by a factor of ~~1.11.~~ 1.13

MARCH 1969

(from *Analog Dialogue*, March, 1969)

The average-responding meter *does* indicate a voltage that is 1.11 (or $\sqrt{2}\ \pi/4$) times the average or rectified value. This is derived from the fact that the average value of a sine wave is 0.637 times the peak and the RMS value is 0.707 times the peak. Thus the meter measures 0.637 and displays 0.707, a ratio of 1.11. This number is, therefore, a calibration constant that must be applied to calculate the effects of waveforms other than sine waves.

For white noise we can show that the average value is $\sqrt{2/\pi}$ times the RMS value. This is derived by integrating the probability distribution of random noise. In the actual measuring instrument, the integration is performed by the ballistics of the meter movement. Therefore, the indication on an average-responding RMS-calibrated meter will be $\sqrt{2/\pi} \times \sqrt{2}\ \pi/4$, which calculates to be 0.886, or −1.05dB. Thus the average-responding meter will indicate 0.886 of the true RMS noise voltage, and its reading must be multiplied by 1.13 to obtain the correct value.

You may wish to refer to the Hewlett-Packard *Journal*, Volume 6, Numbers 8, 9, 10 (*April, May, June, 1955*) for a further discussion of waveform errors in average-responding voltmeters.

Thank you for publishing *Analog Dialogue*. We enjoy reading it very much.

Don A. Wick
Customer Service Manager
Hewlett-Packard
Loveland, Colorado

Our thanks and appreciation to Mr. Wick for his sharp eyes and enlightening comments. If you would like copies of the H-P JOURNAL *issues referred to, we suggest you get in touch with your local H-P field office.*

A professional cartographer, when drawing up a new map, will have it copyrighted. Then he will add into his map a small but distinct error, an artifact.

Any person who steals this map is unlikely to be bright enough to find or correct the error. Wholesale copy of the map including the artifact is acceptable proof of infringement of copyright. The thief is caught with marked bills in his hot hand.

In my NEREM paper on noise[2], I deverly *(sic)* stated that the Fudge Factor to use (when trying to measure white noise on an average-rectified-responding AC voltmeter, with its calibration specified in terms of RMS value of sines) was +11%. *(Ed. The actual figure published in the paper to which Mr. Pease refers was 11.3%)* Actually, the correct value, as stated in our up-to-date applications article P/N-10 is +12.8%, as a thoughtful interpretation of Bennett's *Electrical Noise*[3], page 44, will prove out.

Now, in reference to your recent *Analog Dialogue* article (foot of first column, page 7), tell me there isn't any jam on your face!

Yours for Better Analogs
Robert A. Pease
Philbrick/Nexus Research
Dedham, Massachusetts

Mr. Smith, in his original manuscript, stated: "Most meters will read 12% low when measuring noise, but since this error is constant, a true RMS meter is not required." In converting this figure to a multiplying factor, which is more useful, our slipstick slipped. The correct figure is indeed 1.13, and we confess to having committed a 2% error. But, Mr. Pease, that redness on our face is a blush, not jam!

A further comment: If Mr. Pease is claiming that he has intentionally "rigged" a figure in a paper he has written for presentation at a technical society meeting, for the sole purpose of exposing copyright(?) violations, most readers would wish that it had been an obscure figure, rather than one which is pretty useful. Somehow, this sort of thing is unfair to the engineer who simply wants information, presented as accurately as possible. It also tends to impeach a source whom we know ordinarily to be of high technical integrity, a former colleague for whom we have great admiration. Ours was an honest mistake.

ERRATUM. In *Analog Dialogue*, Vol. 3, No. 1, page 4, Figure 1b, associated with "An op amp and a chopper give precision ramp generator," as reprinted from *Electronic Design*, there is an obvious error:
The 2N1131 transistor should be a PNP type.

[1] *Analog Dialogue*, Volume 3, No. 1, March 1969, "Noise and Operational Amplifier Circuits"
[2] "How to Characterize and Measure Noise in Operational Amplifiers" by R. A. Pease, *NEREM* 1968
[3] *Electrical Noise*, W. R. Bennett, McGraw-Hill

NEW!

RECENT PUBLICATIONS FROM ANALOG DEVICES, INC.

These are a few of the data sheets and application notes that have appeared since the March, 1969 issue. If you are missing one, or if you'd like an extra copy for a colleague, just indicate your wishes on the enclosed card. If your interest runs deeper (if you'd like to try or buy, or just chat with us about any of the items), let us know, and we'd be delighted to get in touch with you.

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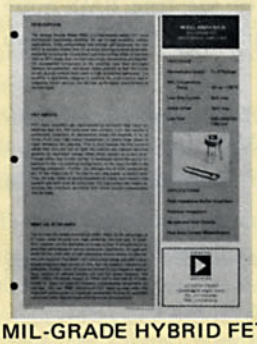

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SPECIFYING MEASURING AND USING VERY HIGH-SPEED D/A CONVERTERS